8-22-00

A

Patent Application

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Oleg Drapkin and Grigory Temkine

Entitled: APPARATUS FOR HIGH DATA RATE SYNCHRONOUS INTERFACE AND METHOD THEREOF

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Dear Sir:

REQUEST FOR FILING A NATIONAL PATENT APPLICATION

Transmitted herewith for filing, please find the following:

_X_ 1. Specification 13 pages, claims 10 pages, and abstract 1 page of the above-referenced patent application.

_X_ 2. 5 sheet(s) of drawing(s) (_X_ formal / ___ informal) comprising Figures 1 through 6 .

_X_ 3. Declaration and executed Power of Attorney's (_X_ signed ___ unsigned).

_____ 3A. No filing fee, Oath, or Declaration is enclosed pursuant to 37 C.F.R 1.53(d).

____ 4. Information Disclosure Statement along with Form PTO-1449 and references.

____ 5. This is a: _____ Continuation-In-Part; _____ Divisional; _____ Continuation; _____substitute Application (MPEP 201.09) of Application Serial No. _____ filed _____; _____ reissue of U.S. Patent No. _____ filed on _____.

An extension to extend the life of the above prior Application to at least the date of filing hereof

(One box must be marked)

(a)_____ is concurrently being filed in that prior Application,

(b)_____ was previously filed in that prior Application,

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____ 6. Attached is an assignment to **ATI International, SRL.** Please return the recorded assignment to the undersigned.

____ 7. Priority is claimed under 35 U.S.C. § 119 based on filing in _____.

	Application No.	Filing Date
(1)	____	____
(2)	____	____
(3)	____	____

____ (No.) Certified copy (copies) ____ are attached; or ____ were previously filed on ____.

____ 8. Attached: ___(No.) verified statement(s) establishing "small entity" status under 37 CFR § 1.9 and 1.27.

__X__ 9. Attached:

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____ 10. Preliminary Amendment:

Prior to a first Office Action, kindly amend the Application as follows:

11. The following Filing Fee calculation is based on the claims filed less any claims canceled by the Preliminary Amendment of Item 10.

					SMALL ENTITY RATE		LARGE ENTITY RATE		
BASIC FEE					$345	OR	$690	=	$690 00
	NUMBER FILED			NUMBER EXTRA					
TOTAL CLAIMS	34	-20	=	14 (at least 0)	x 9	OR	x 18	=	$252.00
INDEP CLAIMS	4	-3	=	1 (at least 0)	x 39	OR	x 78	=	$ 78 00
If any proper multiple dependent claim (ignore improper) is present (Enter $0 00 if this is a reissue application)					+$130	OR	+$260	=	+$____
If assignment is x'd (item 6), add recording fee $40 00									+$ 00.00
Attached is a Rule 47 Petition (inventor refuses to sign or cannot be reached) $130									+$
TOTAL FILING FEE									**=$1,020.00**

_____ 12. A check in the amount of ___ to cover the Filing Fee calculated in Item 11 is attached. Please charge any deficiency or credit any overpayment to ATI Technologies, Inc., Deposit Account No. 50-0441.

__X__ 13. Please charge ATI TECHNOLOGIES, INC., Deposit Account No. 50-0441 in the amount of $1,020.00 the Filing Fee calculated in Item 11. This sheet is attached in duplicate.

__X__ 14. The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and may be required under 37 CFR 1.16-1.18 (missing or insufficiencies only) now or hereafter relative to this application and for the resulting Official Document under 37 CFR 1.20, and to have and cause any necessary petition for extension of time to be filed and any fees necessary to be paid for said extension of time OR credit any overpayment to ATI TECHNOLOGIES, INC. Deposit Account No. 50-0441, for which purpose a duplicate copy of this sheet is attached.

Respectfully submitted,
OLEG DRAPKIN et al

8-21-2000
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PATENT APPLICATION
ATI 000142

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

FILING OF A UNITED STATES PATENT APPLICATION

APPARATUS FOR HIGH DATA RATE SYNCHRONOUS INTERFACE AND METHOD THEREOF

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OUTPUT DRIVER APPARATUS AND METHOD THEREOF

Field of the invention

Present invention relates generally to output drivers, and more specifically to an apparatus and method of dynamically selecting characteristics of the output driver.

Background of the invention

Operating frequencies of semiconductor devices have increased dramatically as new processing technologies have been developed. At high frequencies, the connections between output drivers and input buffers cannot be treated as an electrical short. Instead, the connections between drivers and buffers need to be characterized as a transmission line having a specific impedance. It is well known for output buffers to have an impedance that matches the impedance of the line which it is driving. Known solutions for matching output buffer impedance to transmission line impedance include allowing for output buffers with programmable impedance that can be fixed. For example, an output buffer may have a programmable impedance in the range of 40 to 70 ohms with a resolution of 5 ohms to match a typical transmission line impedance.

While buffers with programmable impedance are useful for matching specific components to a specific system, such impedance matching

techniques do not accommodate variances in transmission line impedance that can occur during high frequency operation. For example, variations in impedance can occur during operation depending upon the specific data pattern been transmitted over one or more data lines because of parasitic capacitance and inductance of the package, as well as because of parasitic capacitance and inductance of the signal traces. An apparatus capable of adjusting the drive strength of output buffers and/or impedance of output buffers to accommodate these dynamic variances in impedance would be useful.

Brief Description of the Drawings

Figure 1 illustrates, in block diagram form, a system in accordance with present invention;

Figure 2 illustrates, in block diagram form, a portion of the drive controller of Figure 1 in greater detail;

Figure 3 illustrates, in block diagram form, a portion of one of the drive controls of Figure 2 in greater detail;

Figure 4 illustrates, in block diagram form, a portion of the dynamic impedance controller of Figure 3 in greater detail;

Figure 5 illustrates, in block diagram form, a portion of one of the drivers of Figure 2 in greater detail; and

Figure 6 illustrates, in block diagram form, a portion of the dynamic driver of Figure 5 in greater detail.

One skilled in the art will appreciate that elements in the Figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the Figures are exaggerated relative to other elements to help to improve understanding of embodiment(s) of the present invention.

Detailed Description of the Drawings

In accordance with a specific embodiment of the present invention, a drive control monitors a dynamic condition to determine when a transmission line impedance is to vary. For example, a specific bit pattern associated with DATA1-DATAn can be monitored by the drive control. Based upon the dynamic condition, the drive control will determine whether the drive strength of output drivers at one or more nodes is to be adjusted. Independently increasing or decreasing drive strengths at the individual output nodes of the drivers compensates for the variance in line impedance. The present invention is better understood with reference to the specific embodiments illustrated Figures 1- 6.

Figure 1 illustrates, in block diagram form, a system 10 in accordance with present invention. The system 10 of Figure 1 includes a first device 12 connected to a second device 16 through interconnects 31-34. Generally, devices 12 and 16 can represent two separate semiconductor devices connected by circuit board interconnect 31-34 (traces), or different portions of a common semiconductor device where the interconnects 31-34 would be conductive traces on the semiconductor device. In one embodiment, the devices 12 and 16 are a data processor and memory respectively. In another

embodiment, the device 12 and 16 are each data processors. The interconnects 31-34 can represent individual data lines associated with a bus. The interconnects 31-34 are illustrated as transmission lines because they can be driven by signals having transition rates that result in a transmission line impedance being observed from the driving device 12.

The device 12 includes a drive control 14 having inputs to receive data signals DATA1-DATAn, and outputs for driving nodes 21-24. Note in other embodiments, the drive control 14 can have bi-directional drivers connected to the nodes 21-24, however, for purposes of discussion, drive controller 14 is treated as having output drivers only.

The static line impedance may be the same or different for each of the transmission lines 31-34. The static line impedance means the line impedance under a predefined condition. For example, for a specific data being transmitted, at a specific drive strength, a static line impedance will be observed.

In one embodiment, the transmission lines 31-34 may be functionally related. For example, they may be individual bit lines of a data bus. In another embodiment, transmission lines 31-34 are not functionally related. For purposes of discussion herein, any traces having adjacent numbers, for example, traces 31 and 32, are considered to be immediately adjacent to one another. For example, the trace 31 is immediately adjacent to trace 32 when they are routed side-by-side with no other traces between them. Traces located immediately adjacent to each other are more susceptible to cross-talk than traces spaced further apart. It will be appreciated that two traces which are side-by-side for a significant length can also be considered immediately

adjacent. In addition to be adjacent in the horizontal plane, it is possible for traces to be adjacent in other planes as well. For example, two traces can be adjacent in the vertical or diagonal plane.

In operation, the dynamic control portion 14 monitors the data values DATA1-DATAn to predict the impedance of each transmission line 31-34 during a next transition. Based upon the predicted value, the drive strength of the buffers that drive lines 31-34 will be adjusted. Generally, if the drive control 14 detects that a specific transmission line impedance is going to increase due to a specific sequence of output bit values (bit pattern), the drive strength of the output buffer driving that specific transmission line will be increased. The higher drive strength helps overcome the effects of increased impedance. Similarly, if the drive control 14 detects that a specific transmission line impedance is going to decrease due to a specific output bit pattern, the drive strength of the output buffer driving that specific transmission line will be decreased.

In a specific embodiment, the dynamic control portion 14 monitors the data values DATA1-DATAn in real time. For a synchronous system real-time indicates that each possible transition time is monitored. For example, if data on a specific data line can change once every clock cycle, the drive control 14 will monitor the data value on that data line at least once every clock cycle. Likewise, the drive control 14 can adjust the output drivers in real-time. The actual adjustment made to the output drivers can be made prior to when the predicted change in impedance is to occur, just after the time when the change in impedance is expected to occur, or prior to and continuing into the time when the change in impedance is expected.

Figure 2 illustrates a portion of the drive control 14 in greater detail and portions of the transmission lines 71-77. Specifically, Figure 2 illustrates output drivers 61-67, and drive controls 51-57. Each of the transmission lines 71-77 is driven by a drive control/driver combination. For example, transmission line 71 is driven by driver 61, which receives data and control signals from the drive control 51. Likewise, driver 61, which receive data and control signals from the drive control 52, drives transmission line 72.

Each of the drive controls 51-57 is connected to receive the data to be driven by its respective driver 61-68, and the data to be driven by the immediately adjacent drivers as well. For example, the signal labeled DATA2 is provided to the adjacent drive controls 51 and 53, as well as to drive control 52. Note that in the specific embodiment of Figure 2, the first and last drive controls, drive control 51 and drive control 57, receive only one adjacent data signal.

Figure 3 illustrates a specific embodiment of one of the drive control blocks 51-57. For purposes of example, Figure 3 is identified as drive control block 52. Specifically, the drive control block 52 includes a static impedance controller 132 and a dynamic impedance controller 134. The dynamic impedance controller 134 receives data to be driven at its own output drive (DATA(N)), as well as the data to be driven by the immediately adjacent output drivers (DATA(N+1) and DATA(N-1)). The dynamic impedance controller 134 monitors the received data values and generates a dynamic control signal based on these values.

The static impedance controller 132 sets the static impedance of the

output driver. Generally, a static impedance controller can be used to set impedance of the driver in the range of 10-110 Ohms. The static impedance controller 132 provides a signal labeled STATIC CONTROL, which is sent to the driver.

Figure 4 illustrates the dynamic impedance controller 134 of Figure 3 in greater detail. Specifically, Figure 4 includes a serial data controller 136 and an adjacent data controller 138.

The serial data controller 136 monitors a serial bit stream of data associated with the output buffer of the controller. The serial bit stream data is stored in a storage location 139. In a specific embodiment, the storage location 139 can be a first-in-first-out memory (FIFO) that stores the data that has been and/or will be driven by the associated driver. In a specific implementation, the FIFO will have a predetermined depth. For example, the FIFO can hold three bits or five bits of data. In other implementations, the depth of the FIFO can be programmable. By having a programmable FIFO depth, higher order effects of previously driven data can be determined. However, it should be understood that the heuristics used to control the drive strength of the output buffer would control the overall complexity of the system.

As illustrated in Figure 4, the serial data controller 136 is connected to three storage locations of memory 139, and generates a control signal labeled SERIAL CONTROL. The SERIAL CONTROL signal is used at the output driver to adjust its drive strengths based upon the serial data stream associated with buffer.

The adjacent data controller 138 monitors adjacent bits of data

associated with the controller 134. The monitored adjacent data can include just the immediately adjacent bits of data, or a plurality of immediately adjacent bits. Higher order cross-talk effects can be taken into account by monitoring a plurality of immediately adjacent bits. However, it should be understood that the complexity of the system would be based upon the heuristics used to control the drive strength. As illustrated in Figure 4, the adjacent data controller 138 generates a signal labeled ADJACENT CONTROL, which is based upon the values of the adjacent data bits, and data to be driven.

The manner in which the data drivers are to be adjusted is better understood with reference to the sample bit pattern illustrated in the table below.

Table 1

(Sample Bit Pattern)

	T0	T1	T2	T3	T4
OUT1	0	0	1	0	0
OUT2	1	1	0	1	0
OUT3	0	0	1	0	1
OUT4	1	1	1	0	1
OUT5	0	0	0	1	0

The rows of the table represent five output drivers OUT1-OUT5. The

columns of the table represent five time cycles T0-T4. The values in the table represent signal values driven by the drivers during the indicated time cycle. The cycles T0-T4 can be either future output values, past output values or a combination of past and future output values.

Table 2

(Sample Bit Pattern)

	T0	T1	T2	T3	T4
OUT1	0	**0**	**1**	0	0
OUT2	1	**1**	**0**	1	0
OUT3	0	**0**	**1**	0	1
OUT4	1	1	1	0	1
OUT5	0	0	0	0	1

The bold portion of Table 2 indicates a parallel portion of the bit pattern that will result in a predicted increase in impedance viewed at the driver OUT2. Specifically, during the transition from time T1 to time T2 the driver OUT2 is driving its data line from a high voltage value to a low voltage value, while the drivers OUT1 and OUT3 are driving their data lines in the opposite direction, i.e. from low voltage values to higher values. This bit pattern scenario can be predicted to result in cross-talk on the data line being driven by driver OUT 2, such that the effective impedance of this line is increased. In order to compensate, the adjacent data controller 138 of Figure 4 detects this condition and provides an ADJACENT CONTROL signal that will increase the drive of driver OUT2 to assure the line it is

driving will be discharged to an appropriate voltage level within the allotted time cycle. Likewise, when the transitions are opposite those highlighted in table 2, i.e. OUT2 is rising while OUT1 and OUIT3 are falling, the impedance of OUT2 can be predicted to increase.

Table 3

(Sample Bit Pattern)

	T0	**T1**	**T2**	**T3**	**T4**
OUT1	0	0	1	0	0
OUT2	1	1	0	1	0
OUT3	0	0	1	0	1
OUT4	**1**	**1**	**1**	**0**	1
OUT5	0	0	0	0	1

Table 3 highlights data being driven at node 4. Specifically, the data is driven to a high voltage for three full cycles before being driven to a low voltage. When a common value is driven high over a trace for a long period of time, the effect is to fully charge the entire trace to a maximum voltage value. When frequently alternating data is being driven on a trace that is acting as a transmission, the trace does not fully charge. The impedance of a transmission line that is fully charged in this case is greater that the impedance of a transmission line that is partially charged. In accordance with a specific embodiment of the present invention, when a trace is fully charged can be predicted. For example, the driver OUT4 has been driven high for cycles T0-T2. In response, the output drive associated with driver

OUT4 can be increased for time T3 to compensate for the increase in effective impedance of the data line. Note that an increase in effective impedance is also observed when a data line is fully driven to a low voltage. The number of cycles that are needed to affect the impedance of a data line (i.e. fully charge or discharge a trace) varies with the frequency of data change. Therefore, in a specific embodiment of the present invention, a user definable frequency indicator can be provided to assist in determining when the drive strengths need to be changed.

Table 4

(Sample Bit Pattern)

	T0	T1	T2	T3	T4
OUT1	0	0	1	0	0
OUT2	1	1	0	1	0
OUT3	0	0	1	**0**	**1**
OUT4	1	1	1	**0**	**1**
OUT5	0	0	0	**0**	**1**

The bold portion of Table 4 indicates a parallel portion of the bit pattern that will result in a predicted decrease in line impedance viewed from the driver OUT4. Specifically, during the transition from time T3 to time T4 the drivers OUT3-OUT5 are each driving their data lines from a low voltage value to a high voltage value. This bit pattern scenario can be predicted to result in cross-talk on the data line being driven by driver

OUT4, such that the effective impedance this line is decreased. In order to compensate, the adjacent data controller 138 of Figure 4 is configured to detect this low impedance condition and to provide an ADJACENT CONTROL signal that will decrease the drive of driver OUT4 to assure the line it is driving will be discharged to an appropriate voltage level within the allotted time cycle. Likewise, when the transitions are opposite those highlighted in table 4, i.e. OUT3-OUT5 are transitioning from high to low, the impedance of OUT4 can be predicted to decrease.

Allowing for dynamic adjustments in drive strength is an advantage over the prior art because it allows for an overall reduction in power and system noise. Prior art buffers had to be designed to assume a worst-case bit pattern scenario, resulting in buffers that had drive strength greater than needed for most scenarios. Allowing for dynamic control drive strength allows the drive strength to be dynamically controlled based upon bit pattern information. Therefore, a reduction in noise and power consumption can be realized by allowing for dynamic monitoring and adjusting of all output buffer drive strengths.

Figure 5 illustrates in greater detail a specific embodiment of a driver, for example driver 62, controlled by the embodiments put forth herein. Specifically, the driver 62 includes a normal driver 151 connected to receive data signal and providing a signal to the output pad, or node. In addition, the driver 62 includes a dynamic driver 152 connected to receive the data signal and to provide a signal to the output pad, or node. In addition, each of the normal driver 151 and the data driver 152 receives at least a portion of control signal as discussed herein.

A static control portion of the control signal, which will set impedance of the driver to a predefined value, controls the normal driver 151. The user usually specifies the predefined value based upon the system specifications. In one embodiment, the normal driver 151 can be programmed to have impedance in a range of 10 to 110 ohms. The dynamic driver 152 receives a dynamic control signal portion from the control signal. The drive strength of the dynamic driver 152 various based upon the dynamic control signal as described herein.

Figure 6 illustrates a specific implementation of the dynamic driver 157. In the specific implementation illustrated, the driver 156 and driver 157 each receive a DATA signal to be driven, and are coupled at their outputs to provide an output signal to the output node. The output buffer 156 is controlled by a signal labeled CTL0 and the output buffer 157 is controlled by signal labeled CTL1. In one embodiment, the driver 156 drives the output during normal operation, while the buffer 157 is turned off. When the dynamic control portion 134 of the driver control 14 determines that additional drive is needed, the signal CTL1 is asserted to turn on driver 157. Note additional drive includes both sinking and sourcing of current. When it is determined that less drive is needed, the signal CTL0 will be deasserted to turn off driver 156, thereby providing less drive. One skilled in the art will recognize that additional drivers can be used in order to provide a greater degree of resolution invariant drive strength.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims

below. For example, the control logic that monitors and changes the drive strengths can be enabled or disabled. In addition, specific monitoring criteria can be enabled, or specified by the user, and can be different for each node. For example, a driver driving the last bit of a data bus may not need dynamic drive adjustments. Also, where a device is driving data lines on a circuit board, it may be desirable for a user to specify which lines each driver's control module is to monitor (i.e. which lines are adjacent). Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense and all such modifications are intended to be included within the scope of present invention. The claims means-plus-function clause(s), if any, cover the structures described herein that perform the recited function(s). The mean-plus-function clause(s) also cover structural equivalents and equivalent structures that perform the recited function(s). Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims.

Claims

We claim:

1. A method comprising the step of:

   monitoring a dynamic condition that causes transmission line impedance to vary;

   dynamically determining based upon the dynamic condition if a drive strength of a first output coupled to a first node is to be adjusted; and

   dynamically adjusting the drive strength of the first output when the step of determining indicates the first output is to be adjusted.

2. The method of claim 1 wherein:

   the step of monitoring the dynamic condition includes monitoring a first plurality of values to be provided substantially simultaneously in time to a plurality of first nodes that are adjacent to the first output; and

   the step of dynamically adjusting includes dynamically adjusting the drive strength of the first output based on the first plurality of values.

3. The method of claim 2, wherein the step of dynamically adjusting includes:

reducing the drive strength of the first output when a signal at the first output is transitioning from a first voltage level to a second voltage level and a majority of the plurality of first nodes is also transitioning from the first voltage level to the second voltage level.

4. The method of claim 3, wherein the majority of first nodes include immediately adjacent nodes.

5. The method of claim 4, wherein the majority of first nodes include two immediately adjacent nodes.

6. The method of claim 2, wherein the step of dynamically adjusting includes:

increasing the drive strength of the first output when a signal at the first output is transitioning from a first voltage level to a second voltage level and a majority of the plurality of first nodes is transitioning from the second voltage level to the first voltage level.

7. The method of claim 1, further comprising the steps of:

dynamically determining based upon the dynamic condition if an output drive strength of a second output coupled to a second node is to be adjusted, wherein determining if the output drive strength of the second output is to be adjusted is independent of determining if the output drive strength of the first output is to be adjusted; and

dynamically adjusting the drive strength of the second output when the step of determining indicates the second output is to be adjusted.

8. The method of claim 7, wherein:

the step of monitoring the dynamic condition includes monitoring a first plurality of values to be provided substantially simultaneously in time to a plurality of first nodes that are adjacent to the first output; and

the step of dynamically adjusting includes dynamically adjusting the drive strength of the first output based on the first plurality of values.

9. The method of claim 8 wherein:

the step of monitoring the dynamic condition includes monitoring a second plurality of values to be provided substantially simultaneously in time to a plurality of second nodes that are adjacent to the second output; and

the step of dynamically adjusting includes dynamically adjusting the drive strength of the second output based on the second plurality of values.

10. The method of claim 9, wherein the nodes of the plurality of first nodes are mutually exclusive of the nodes of the plurality of second nodes.

11. The method of claim 9, wherein the plurality of first nodes includes the second node.

12. The method of claim 11, wherein the plurality of second nodes includes the first node.

13. The method of claim 11, wherein the first node is immediately adjacent to the second node.

14. The method of claim 1, wherein the step of dynamically determining includes determining for each transition of the first output if the output impedance of the first output is to be adjusted.

15. The method of claim 1 wherein:

the step of monitoring the dynamic condition includes monitoring a first plurality of values provided sequentially in time to the first output; and further including

the step of dynamically adjusting includes dynamically adjusting the impedance of the first output based on the first plurality of values.

16. The method of claim 2, wherein the step of dynamically adjusting includes:

increasing the drive of the first output when a signal at the first output is transitioning to a first voltage after having been at a second voltage state for two or more data cycles.

17. A method comprising the steps of:

monitoring a bit pattern set associated with a first output;

dynamically determining based upon the bit pattern set if an output impedance of the first output is to be adjusted; and

dynamically adjusting the impedance of the first output when the step of determining indicates the first output is to be adjusted.

18. The method of claim 17 wherein the steps of dynamically determining and dynamically adjusting occur in real-time.

19. The method of claim 17 wherein the steps of dynamically determining and dynamically adjusting occur for each output cycle of the first output.

20. The method of claim 17 further comprising the step of:

providing to the first output a representation of a portion of the bit pattern set after the step of dynamically adjusting the impedance.

21. The method of claim 17, wherein the first output includes an output bus having a plurality of output drivers.

22. The method of claim 21, wherein the step of dynamically adjusting includes adjusting the impedance of each of the plurality of output drivers independent of the impendence of each of the other plurality of output drivers.

23. The method of claim 21:

wherein the bit pattern set includes at least one serial bit pattern subset, wherein a serial bit pattern subset includes a plurality of data bits to be provided to one of the plurality of output drivers in a time sequential manner.

24. The method of claim 23 wherein:

the bit pattern set includes at least one parallel bit pattern subset, wherein a parallel bit pattern subset includes a plurality of data bits that are provided to a plurality of output drivers during a common output cycle.

25. The method of claim 24, wherein the step of dynamically adjusting includes:

dynamically adjusting the impedance of the first output based upon the serial bit pattern subset and the parallel bit pattern subset when the step of determining indicates the first output is to be adjusted.

26. The method of claim 24, wherein the plurality of output drivers is immediately adjacent output drivers.

27. A method comprising the steps of:
    monitoring a bit pattern set, wherein the bit pattern set is to be provided at an output node; and
    adjusting an impedance of the output node based upon the bit pattern set.

28. The method of claim 27, further comprising the step of:
    determining a depth of the bit pattern set.

29. The method of claim 28, wherein the depth of the bit patterns set is at least partially determined by the length of a line to be connected to the output node.

30. A method comprising the steps of:

monitoring a bit pattern set, wherein the bit pattern set is to be provided in parallel to a plurality of output nodes; and

adjusting an impedance of a first output node of the plurality of output nodes in a first manner based upon the bit pattern set.

31. An apparatus comprising:

a storage element having an input and an output, the storage element for storing a bit pattern set associated with output values; and

a dynamic drive controller having an input coupled the input of the storage element, and an output, wherein a drive strength at the output is based upon the bit pattern.

32. The apparatus of claim 31, wherein the bit pattern is associated with values that are output in parallel.

33. The apparatus of claim 32, wherein the bit pattern is associated with values that are output in serial.

34. The apparatus of claim 31, wherein the bit pattern is associated with values that are output in parallel.

Abstract of The Disclosure

A drive controller monitors a dynamic condition to determine when a transmission line impedance is to vary. In one embodiment, a specific bit pattern associated with a set of data lines can be monitored by the drive controller. Based upon the dynamic condition, the drive controller will determine whether or not the drive strengths of the output drivers associated with the data lines are to be adjusted. The variance in line is compensated for by independently increasing or decreasing drive strengths at the individual output nodes of the drivers.

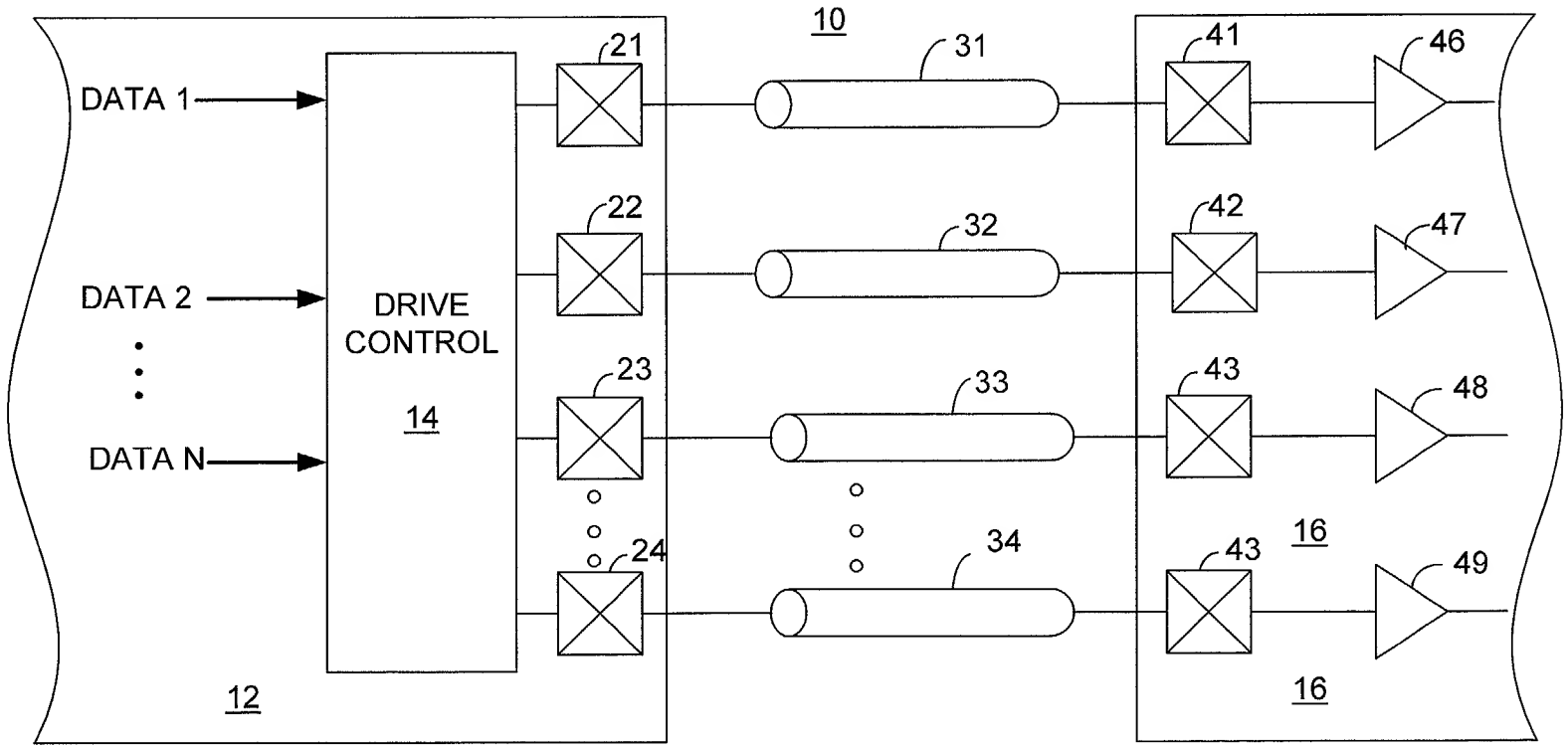


FIGURE 1

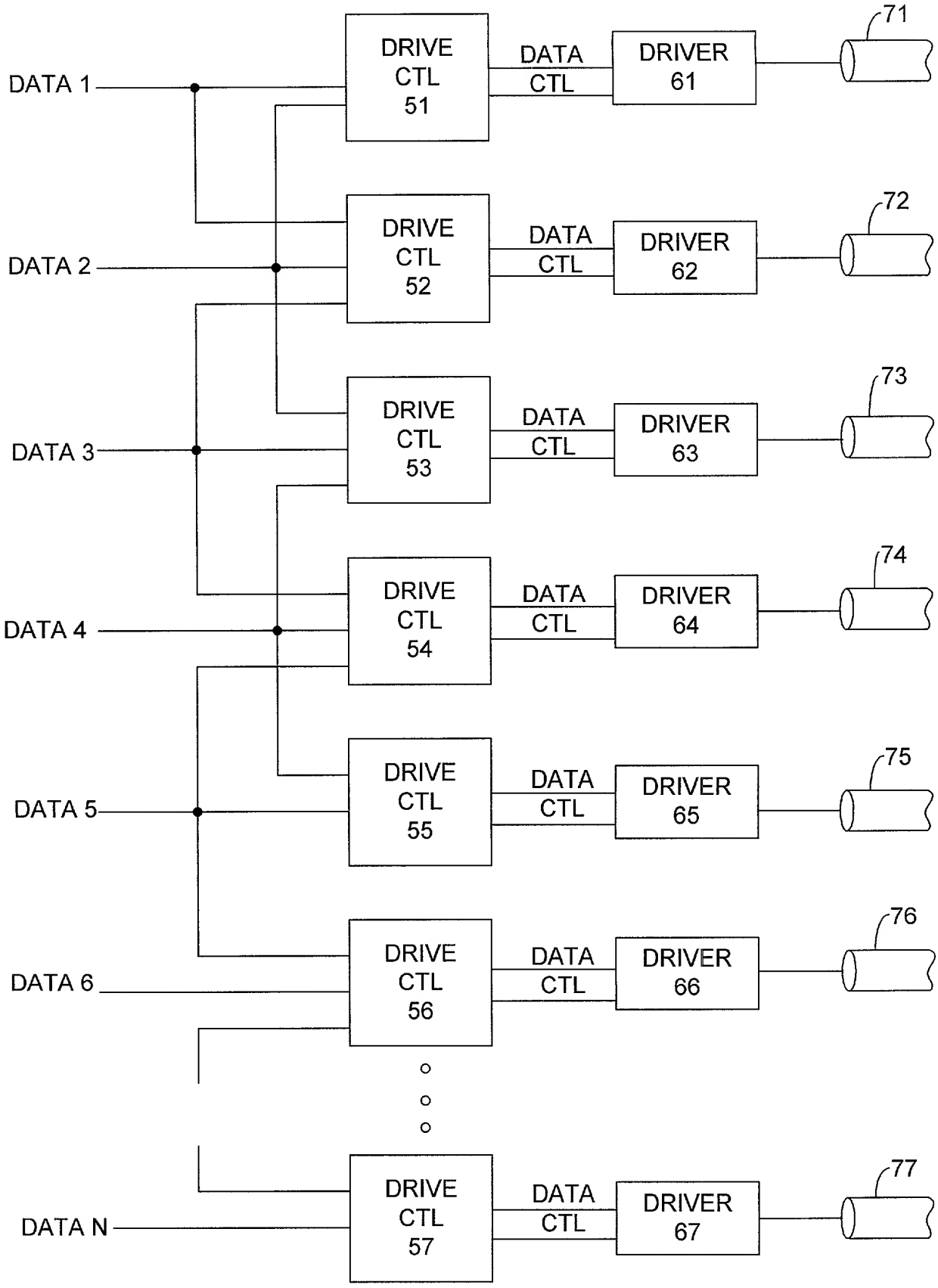

DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA N
DRIVE CTL 51
DRIVE CTL 52
DRIVE CTL 53
DRIVE CTL 54
DRIVE CTL 55
DRIVE CTL 56
DRIVE CTL 57
DATA CTL
DRIVER 61
DRIVER 62
DRIVER 63
DRIVER 64
DRIVER 65
DRIVER 66
DRIVER 67
71
72
73
74
75
76
77

FIGURE 2

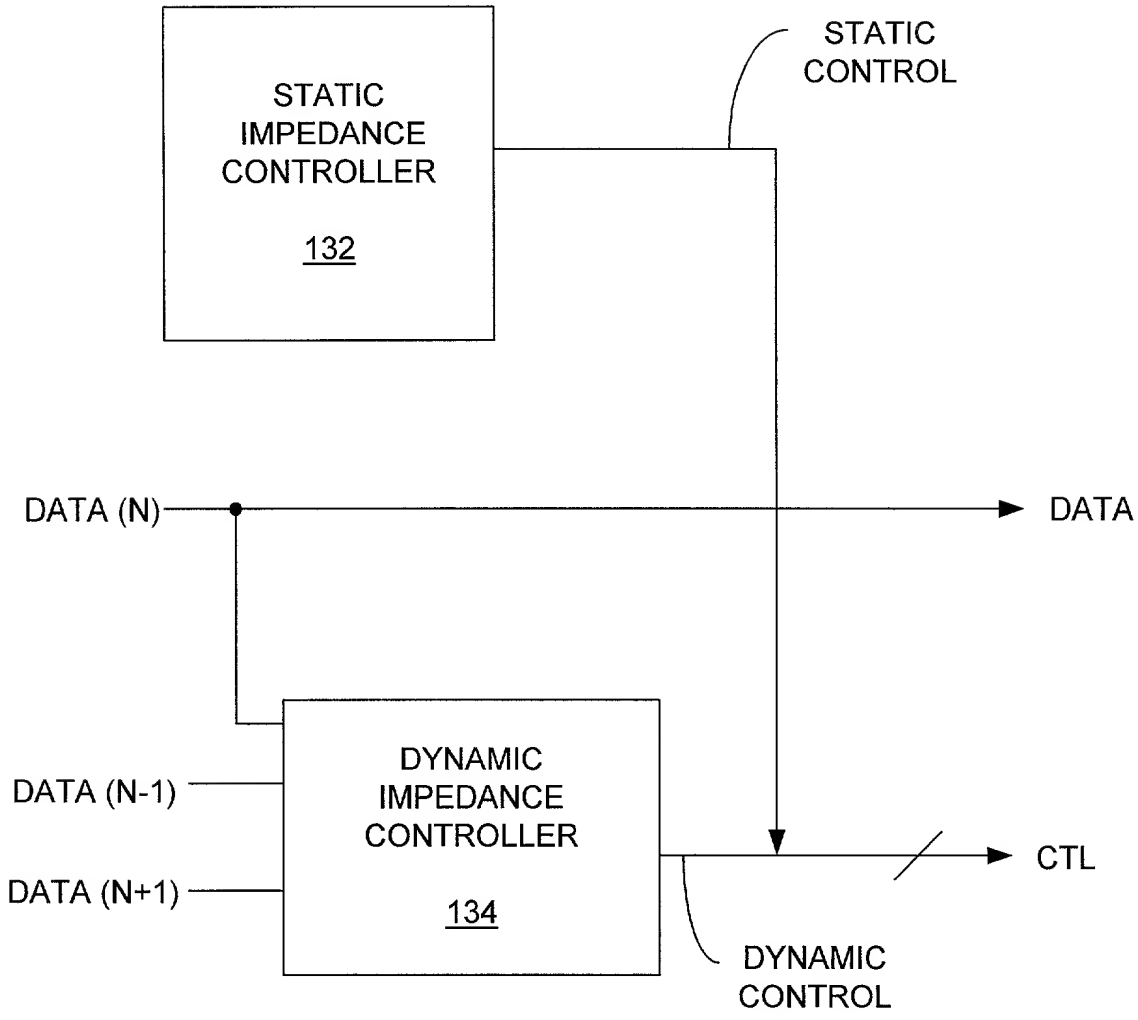

STATIC
IMPEDANCE
CONTROLLER
132
STATIC
CONTROL
DATA (N)
DATA
DATA (N-1)
DATA (N+1)
DYNAMIC
IMPEDANCE
CONTROLLER
134
CTL
DYNAMIC
CONTROL

FIGURE 3

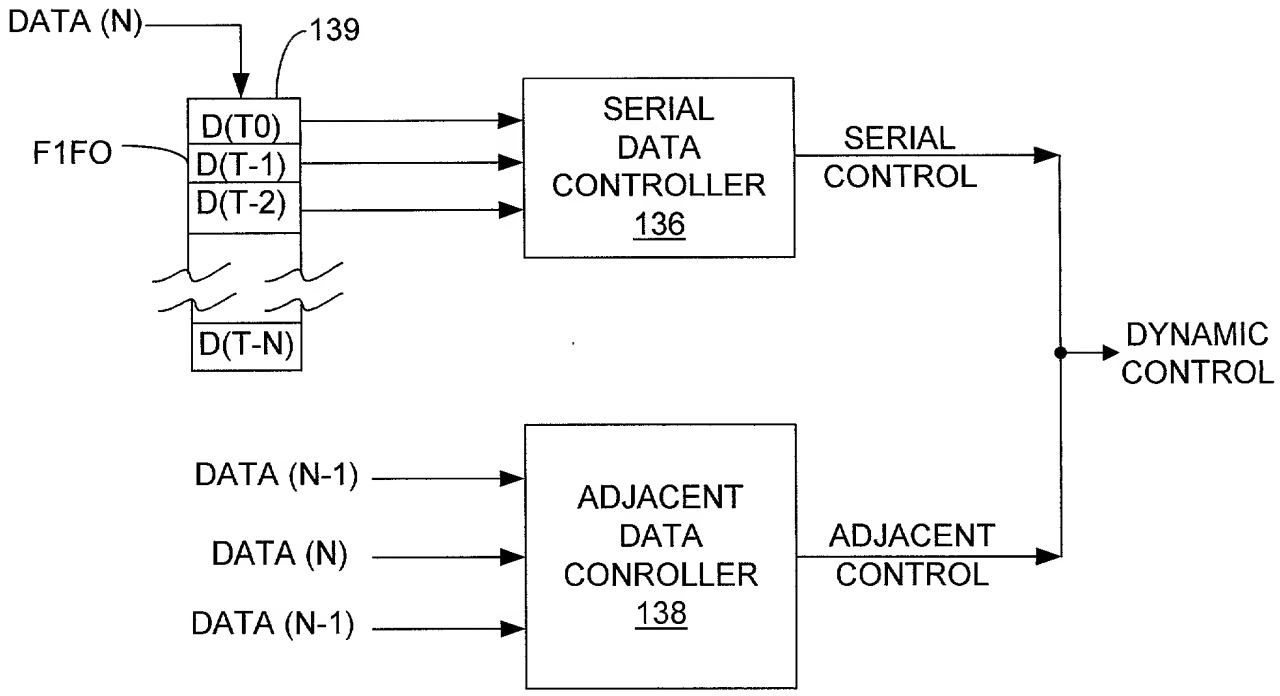


FIGURE 4

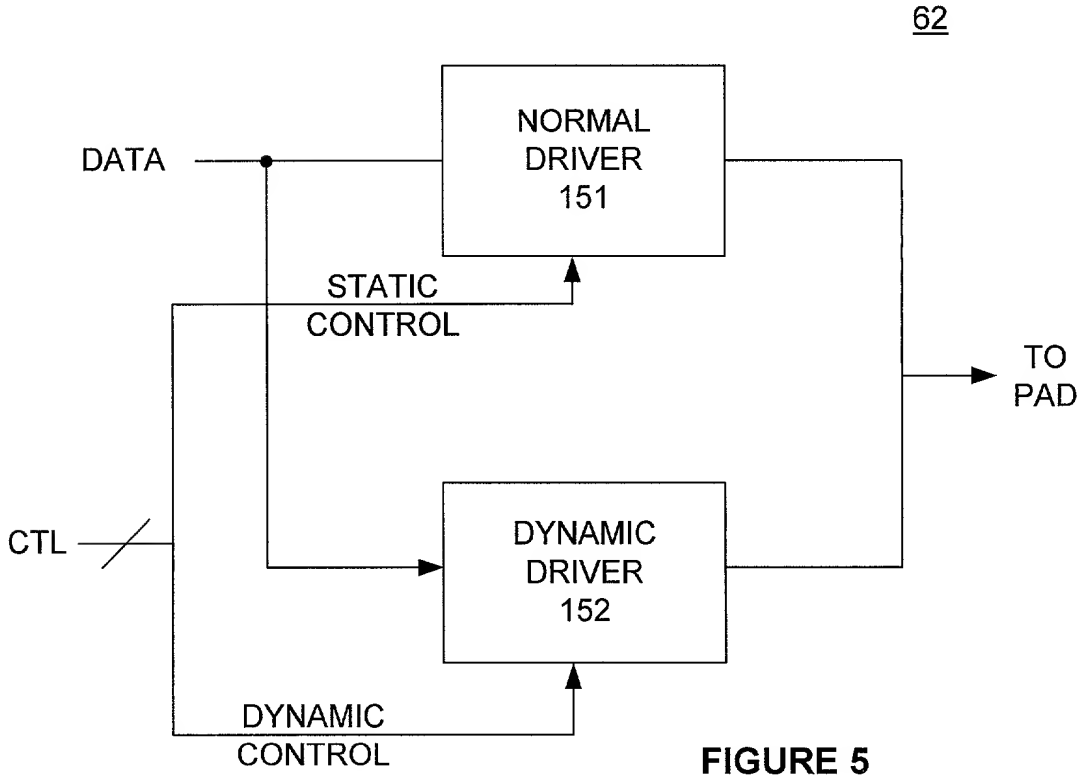


FIGURE 5

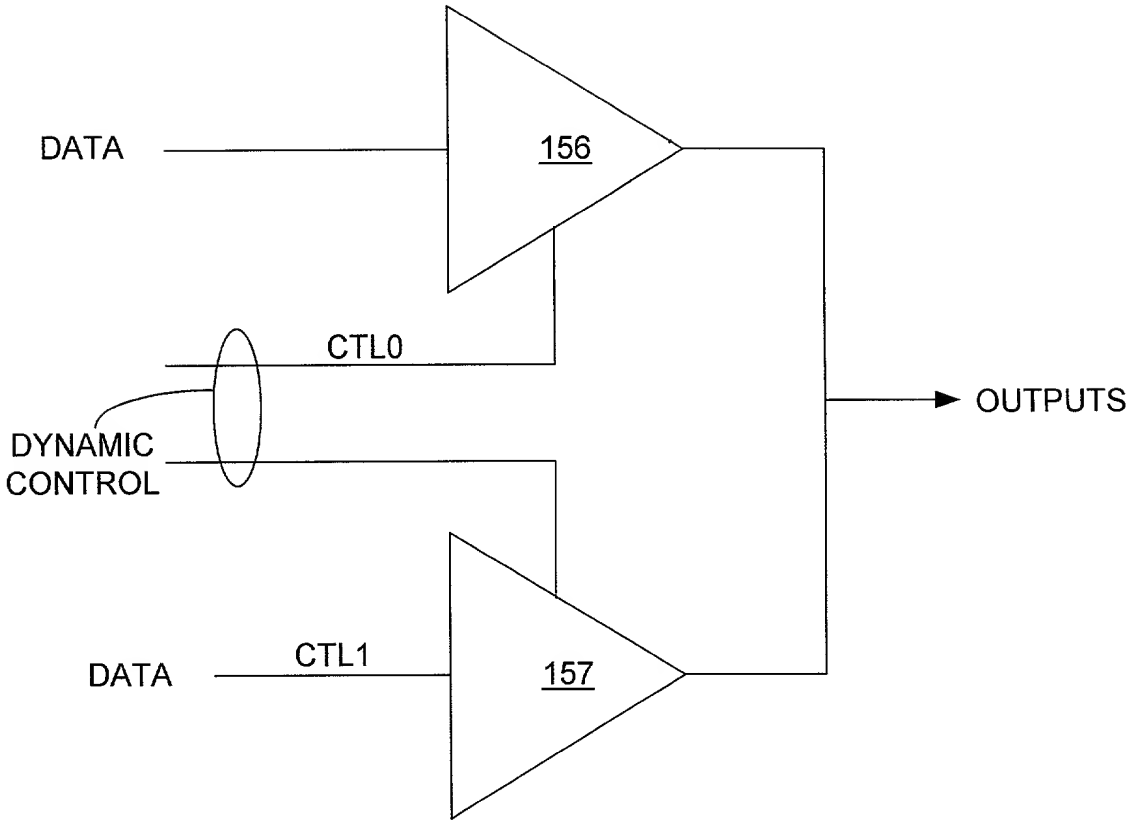


FIGURE 6

Docket #: ATI000142

RULES 63 AND 67 (37 C.F.R. 1.63 and 1.67)
DECLARATION AND POWER OF ATTORNEY

FOR UTILITY/DESIGN/CIP/PCT NATIONAL APPLICATIONS

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; and

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **APPARATUS FOR HIGH DATA RATE SYNCHRONOUS INTERFACE AND METHOD THEREOF**, the specification of which: (mark only one)

X	(a)	is attached hereto.
_____	(b)	was filed on XXXXXXXX as Application Serial No. XXXXXXXXXX and was amended on _____ (if applicable)
_____	(c)	was filed as PCT International Application No. _____ on and was amended on _____ (if applicable).
_____	(d)	was filed on _____ as Application Serial No. ____ and was issued a Notice of Allowance on _____.
_____	(e)	was filed on _____ and bearing attorney docket number _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above or as allowed as indicated above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this application as defined in 37 CFR § 1.56. If this is a continuation-in-part (CIP) application, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose to the Office all information known to me to be material to patentability of the application as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this CIP application.

Docket #: ATI000142

I hereby claim foreign priority benefits under 35 U.S.C. § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which my priority is claimed or, (2) if no priority is claimed, before the filing date of this application:

PRIOR FOREIGN PATENTS						
Number	Country	Month/Day/Year Filed	Date first laid-open or Published	Date patented or Granted	Priority Claimed Yes	No

I hereby claim the benefit under 35 U.S.C. § 120/365 of any United States application(s) listed below and PCT international applications listed above or below:

PRIOR U.S. OR PCT APPLICATIONS

Application No. (series code/serial no.)	Month/Day/Year Filed	Status(pending, abandoned, patented)
XXXXXXXX	XXXXXXXX	XXXXXXX

I hereby appoint Sally Daub, Reg. No. 41,478, and J. Gustav Larson, Reg. No. 39,263 as my attorneys and/or agents, with full power of substitution and revocation, to prosecute this application, provisionals thereof, continuations, continuations-in-part, divisionals, appeals, reissues, substitutions, and extensions thereof and to transact all business in the United States Patent and Trademark Office connected therewith.

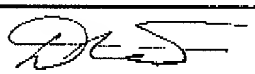
Please address all correspondence and direct all telephone calls to:

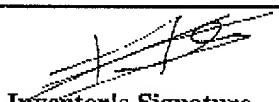
J. Gustav Larson
Simon, Fakhoury, Tangalos, Frantz & Galasso, PLC
P.O. Box 26503
Austin, Texas 78755-0503
Telephone: (512) 372-8240
Facsimile: (512) 372-8247

Docket #: ATI000142

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAMED INVENTOR(S)

1	Oleg Drapkin **Full Name**	 **Inventor's Signature**	14.08.00 **Date**
	341 Brookside Road Richmond Hill, Ontario L4C 0G6, Canada **Residence** (city, state, country)		Canadian **Citizenship**
	Same as Residence Address **Post Office Address** (include zip code)		

2	Grigory Temkine **Full Name**	 **Inventor's Signature**	14.08.00 **Date**
	125 Neptune Dr. #404 Toronto, Ontario M6A 1X3, Canada **Residence** (city, state, country)		Canadian **Citizenship**
	Same as Residence Address **Post Office Address** (include zip code)		

(FOR ADDITIONAL INVENTORS, check here ____ and add additional sheet for inventor information regarding signature, name, date, citizenship, residence and address)